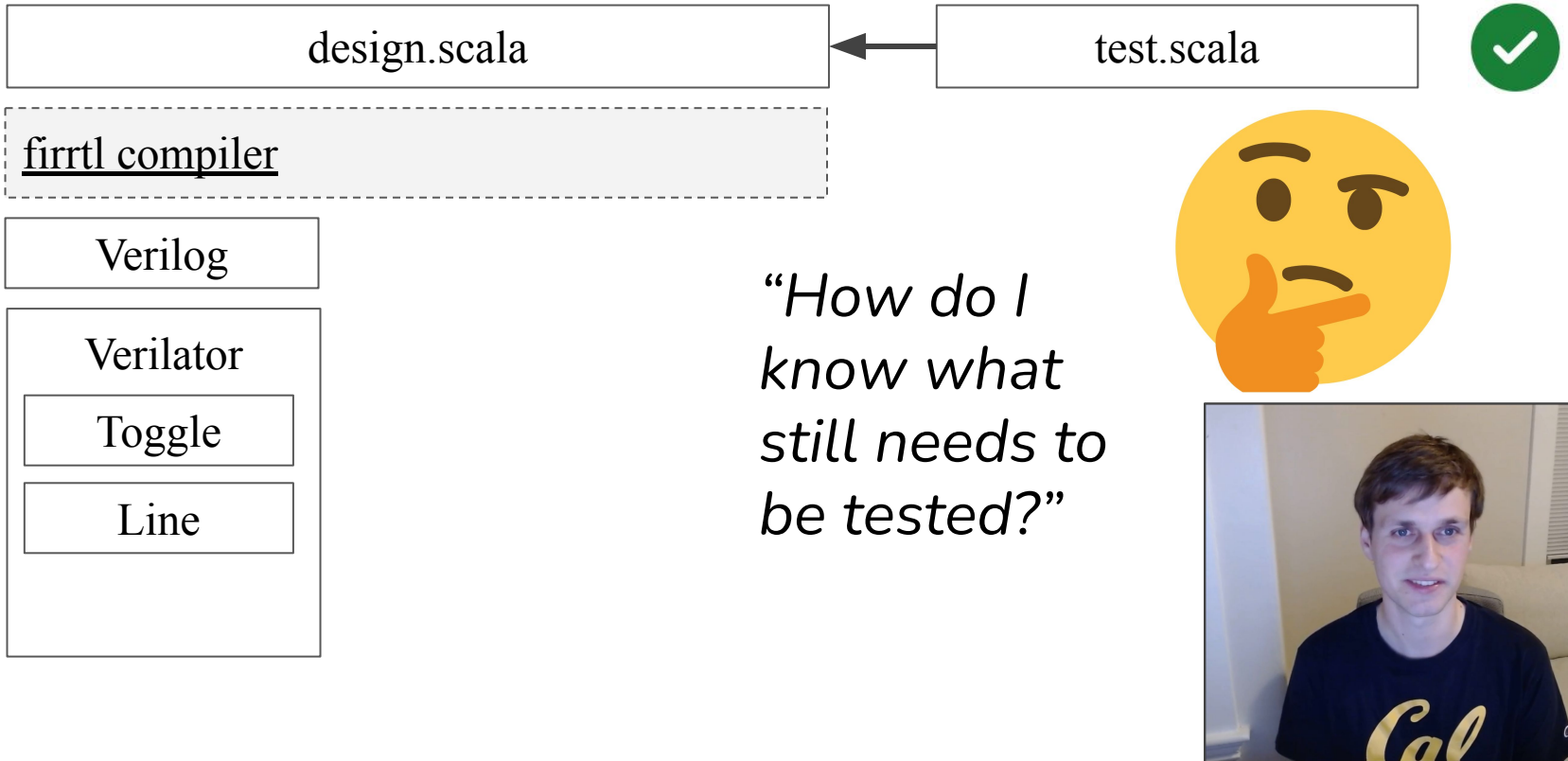
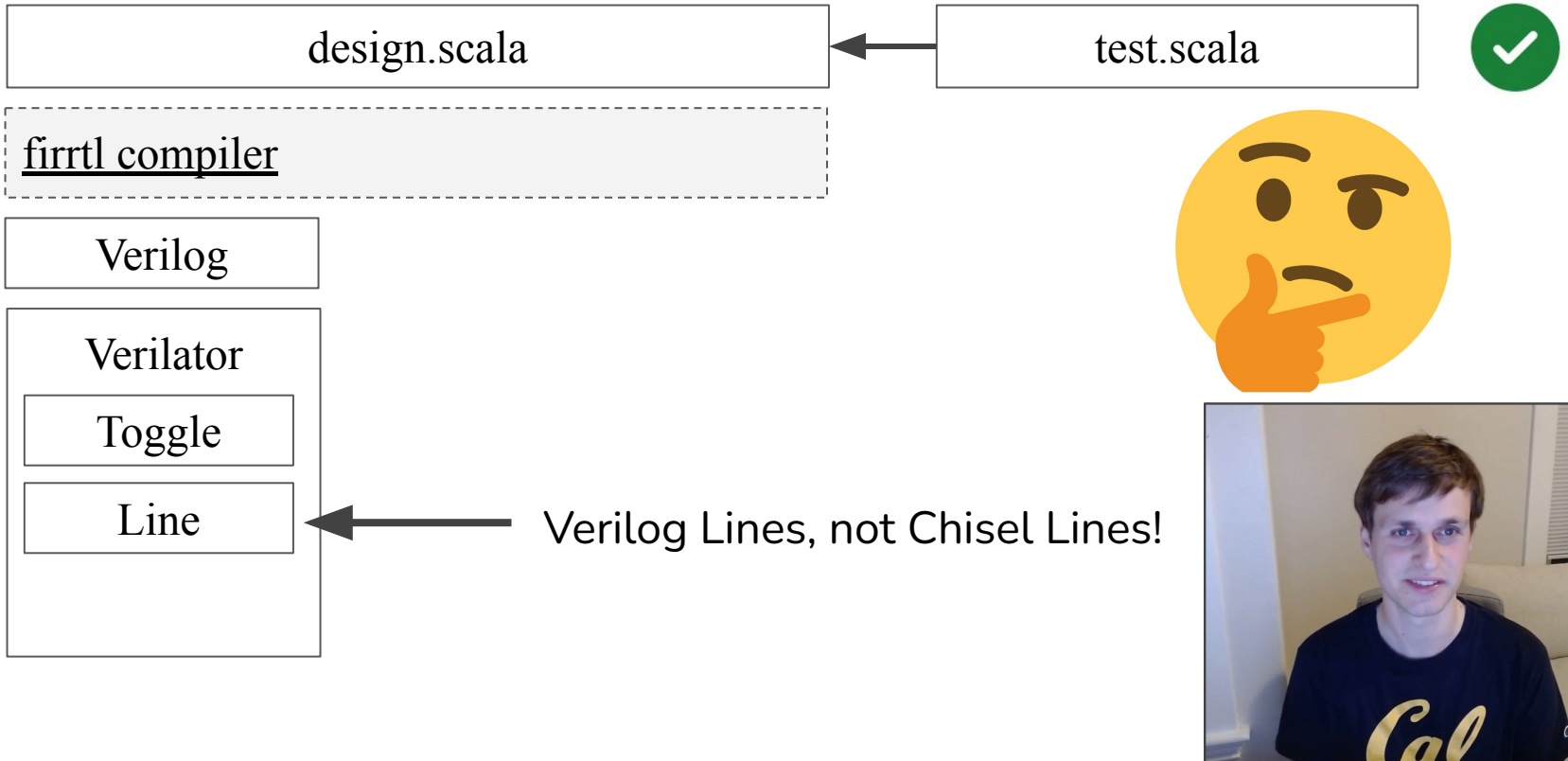
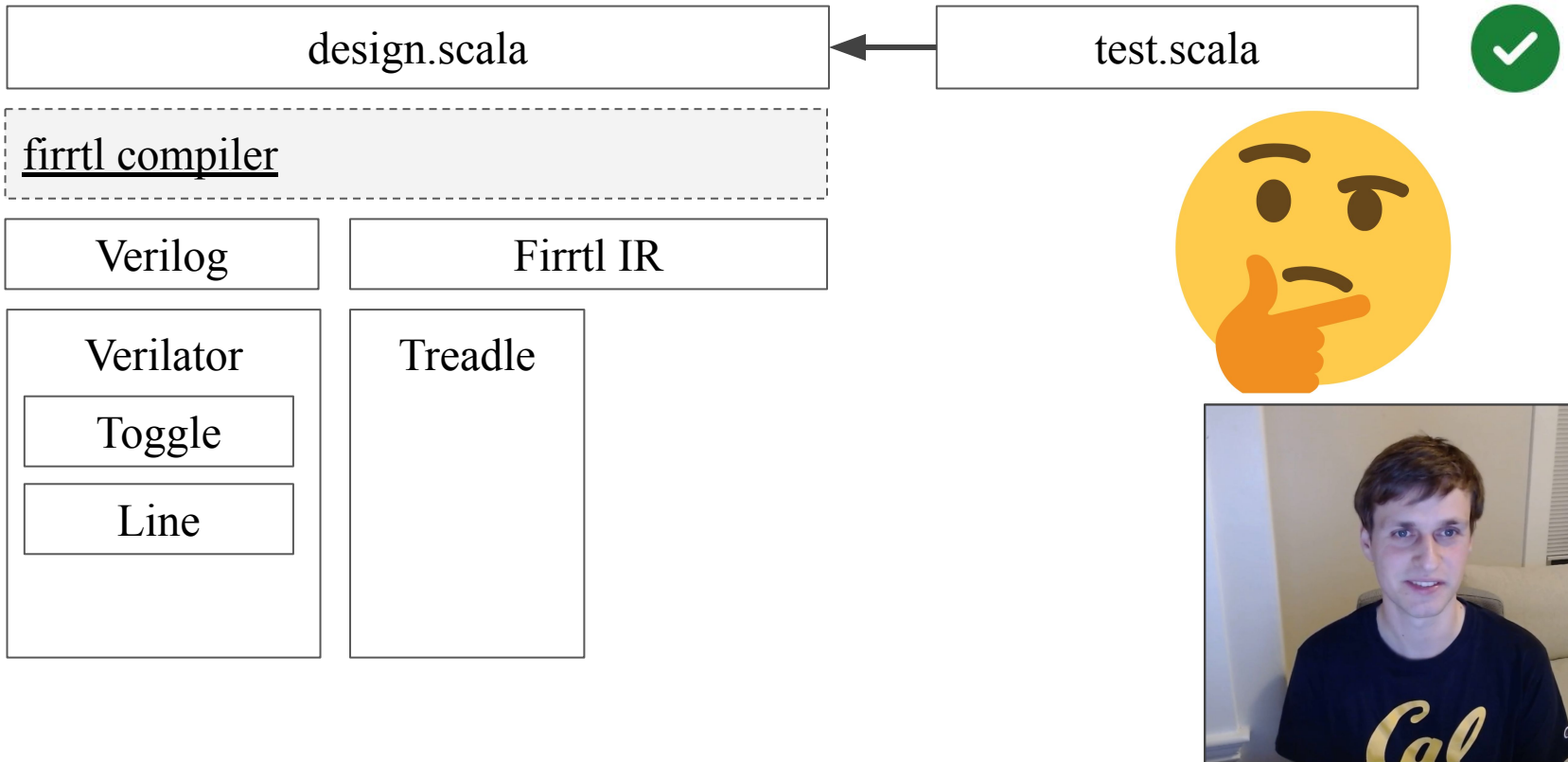
design.scala

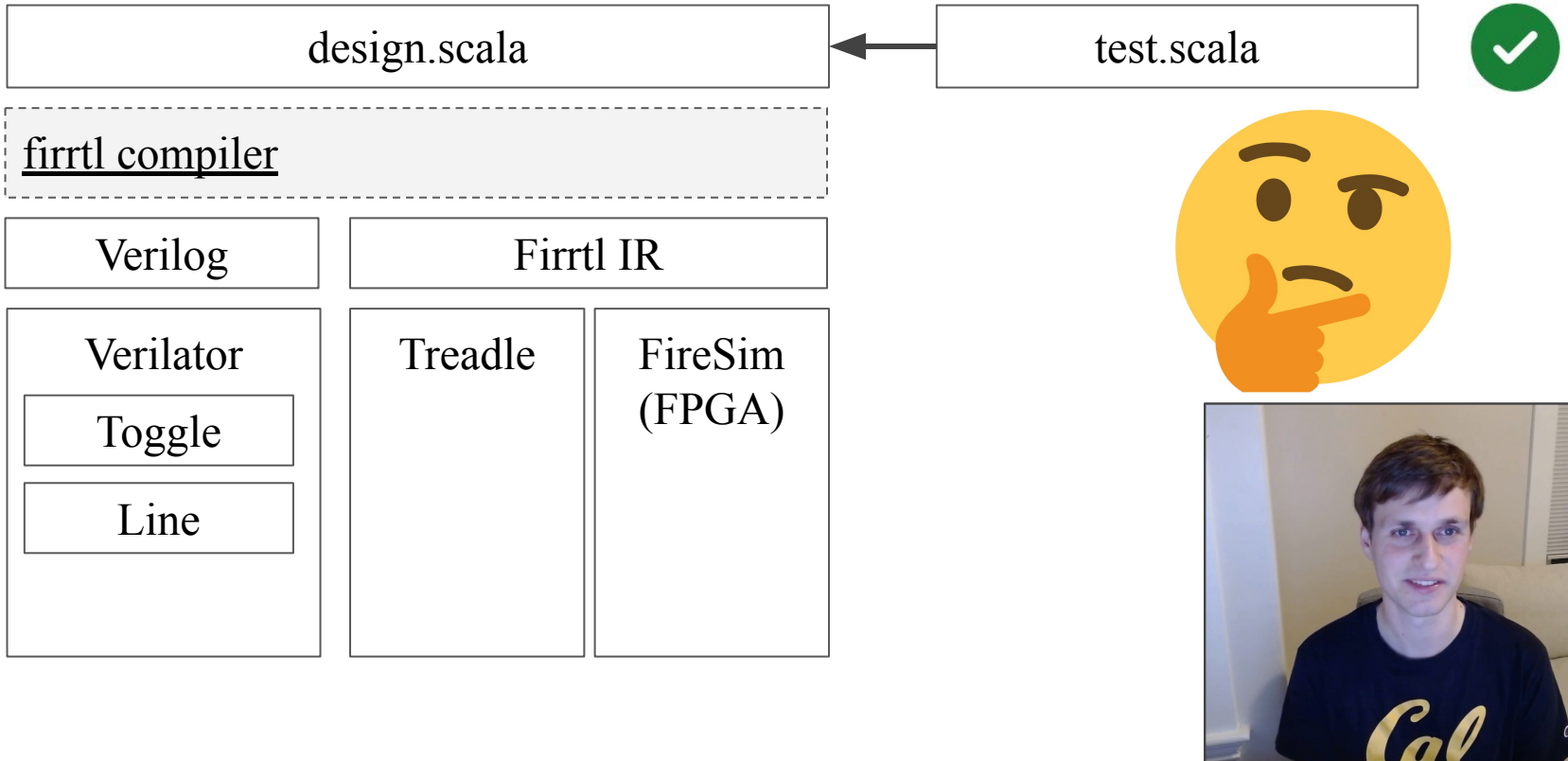

design.scala
test.scala

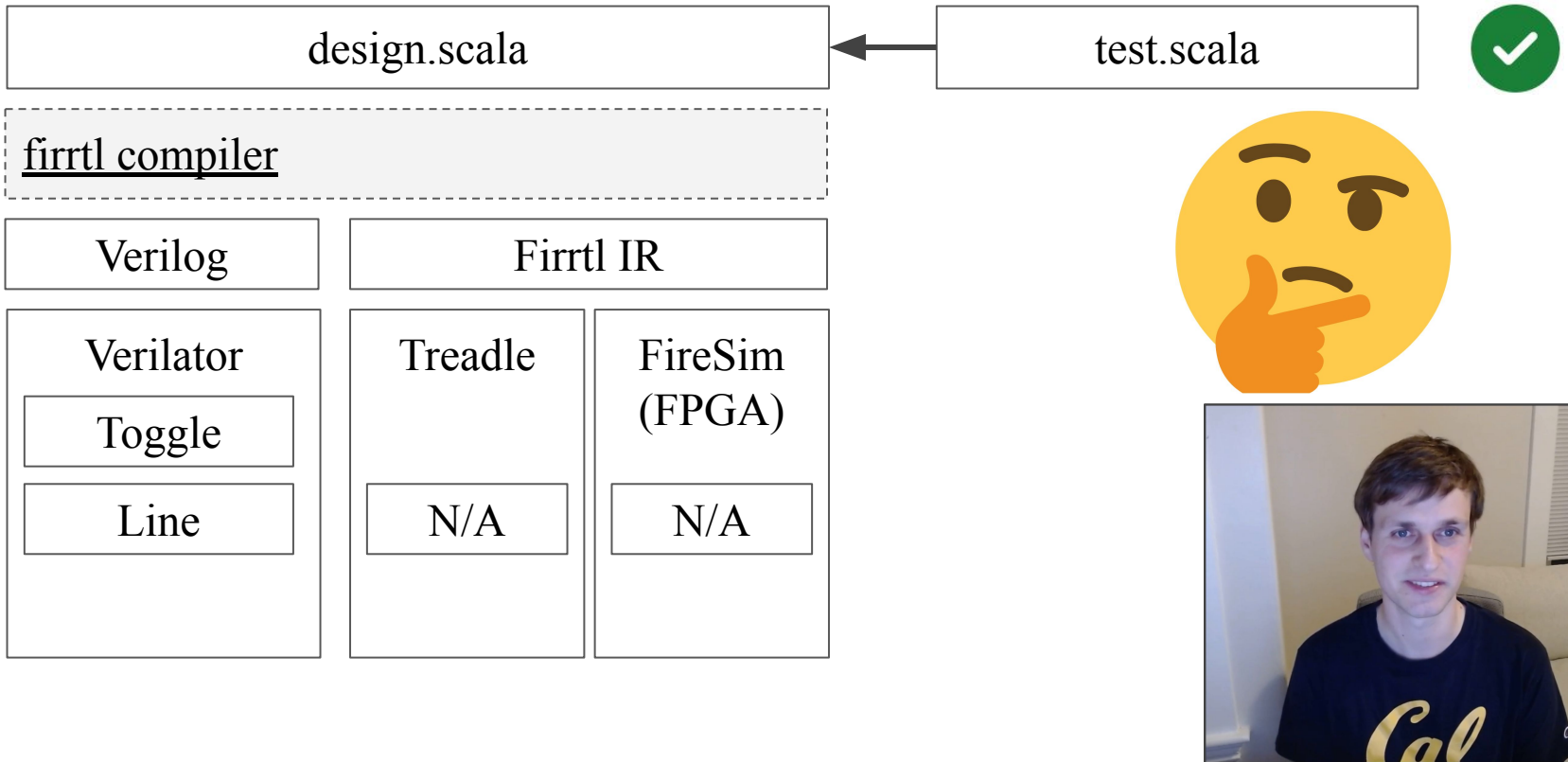
“How do I know what still needs to be tested?”

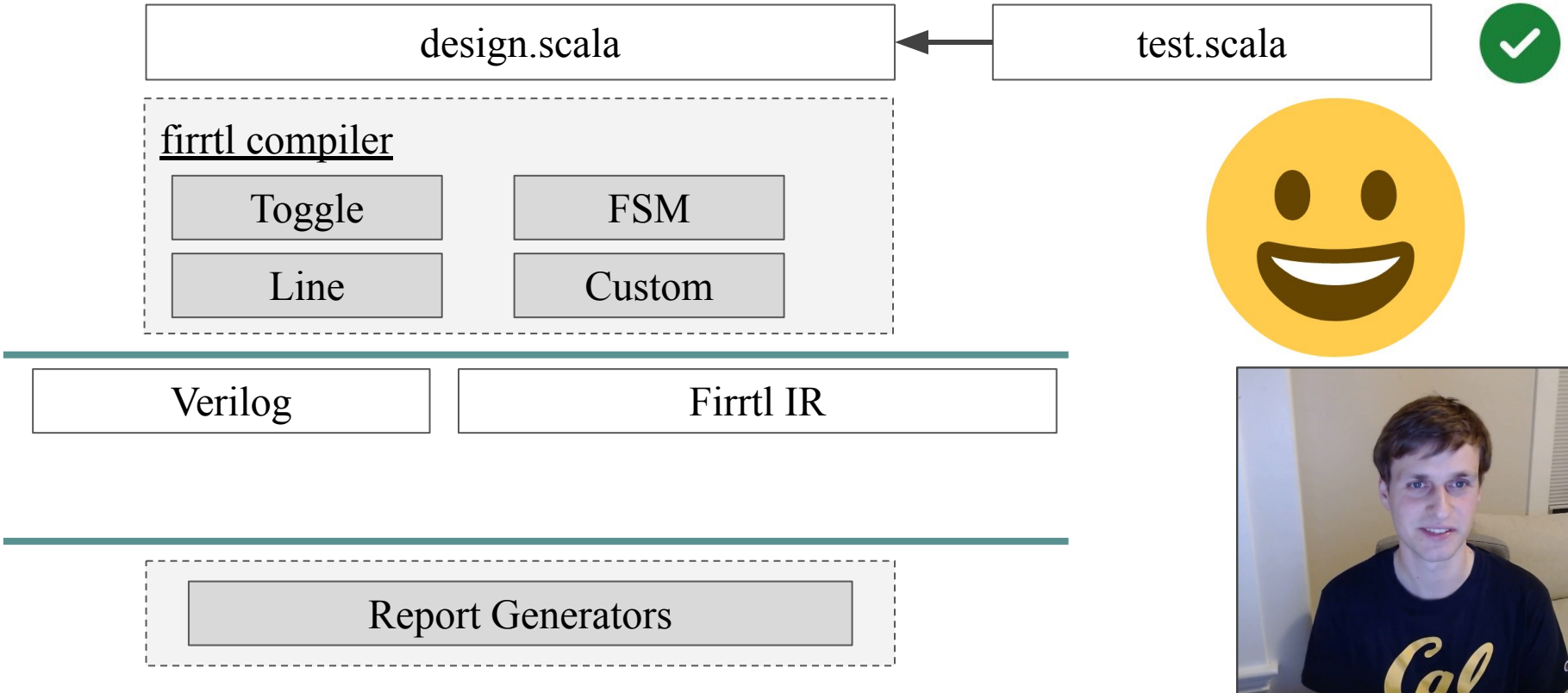

design.scala
test.scala
firrtl compiler
Verilog
Verilator
Toggle
Line
"How do I know what still needs to be tested?"

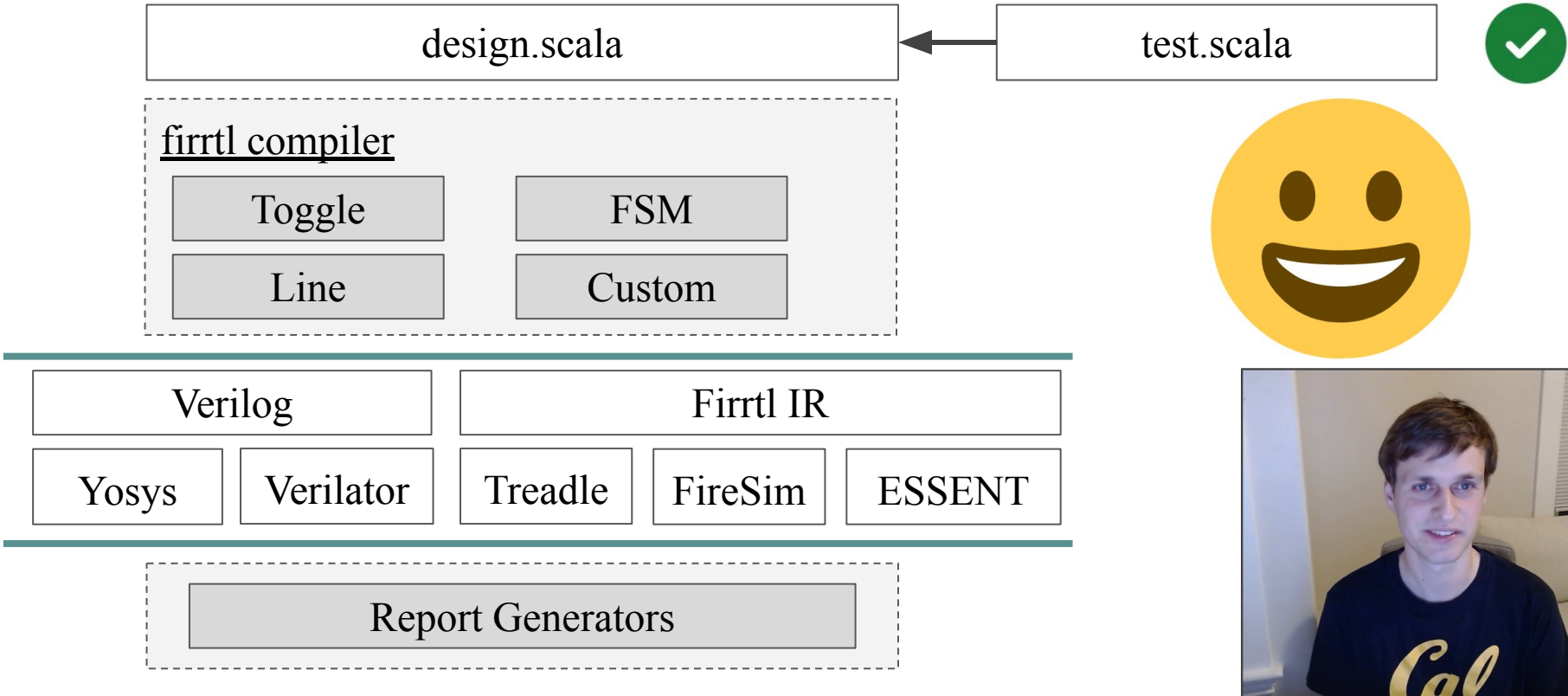

design.scala
test.scala
firrtl compiler
Verilog
Verilator
Toggle
Line
Verilog Lines, not Chisel Lines!


design.scala
test.scala
firrtl compiler
Verilog
Firrtl IR
Verilator
Toggle
Line
Treadle


design.scala
test.scala
firrtl compiler
Verilog
Firrtl IR
Verilator
Toggle
Line
Treadle
FireSim
(FPGA)


design.scala
test.scala
firrtl compiler
Verilog
Firrtl IR
Verilator
Toggle
Line
Treadle
N/A
FireSim
(FPGA)
N/A


design.scala
test.scala
firrtl compiler
Toggle
FSM
Line
Custom
Verilog
Firrtl IR
Report Generators


design.scala
test.scala
firrtl compiler
Toggle
FSM
Line
Custom
Verilog
Firrtl IR
Yosys
Verilator
Treadle
FireSim
ESSENT
Report Generators

Applicable to other hardware languages!

design.~~scala~~ ← test.~~scala~~

your ~~firrtl~~ compiler

- Toggle
- FSM
- Line
- Custom

- Verilog
- Your ~~Firrtl~~ IR

- Yosys
- Verilator
- Treadle
- FireSim
- ESSENT

- Report Generators

Applicable to other hardware languages!

Feedback-Directed Fuzz Testing!

design.scala

test.scala

firrtl compiler

- Toggle
- FSM
- Line
- Custom

Verilog

Firrtl IR

Yosys | Verilator | Treadle | FireSim | ESSENT

Report Generators

Simulator Independent Coverage for RTL Hardware Languages

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Paper PDF

Code on Github

Join us at
Session 4A
Tuesday
10:20 am