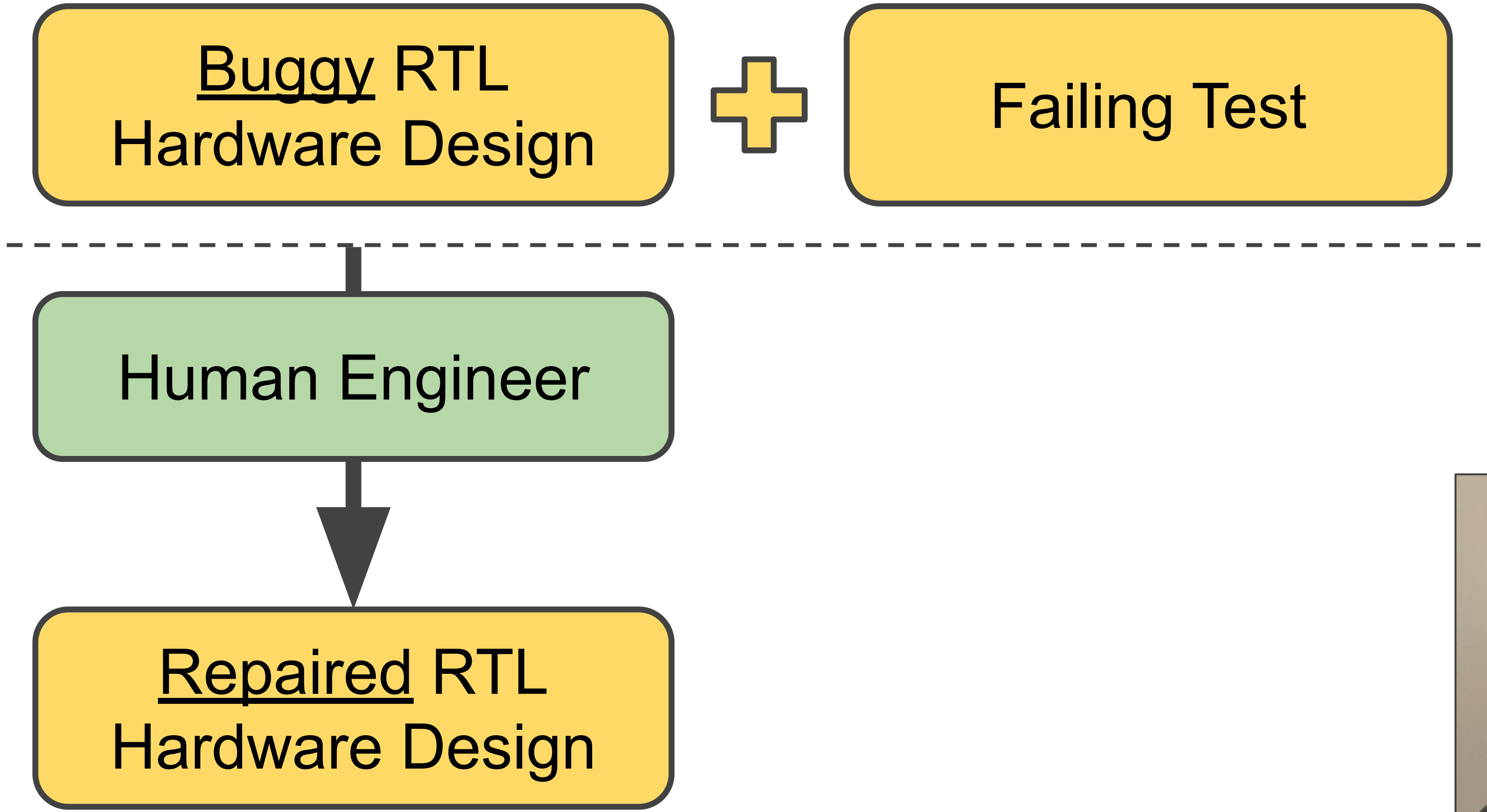
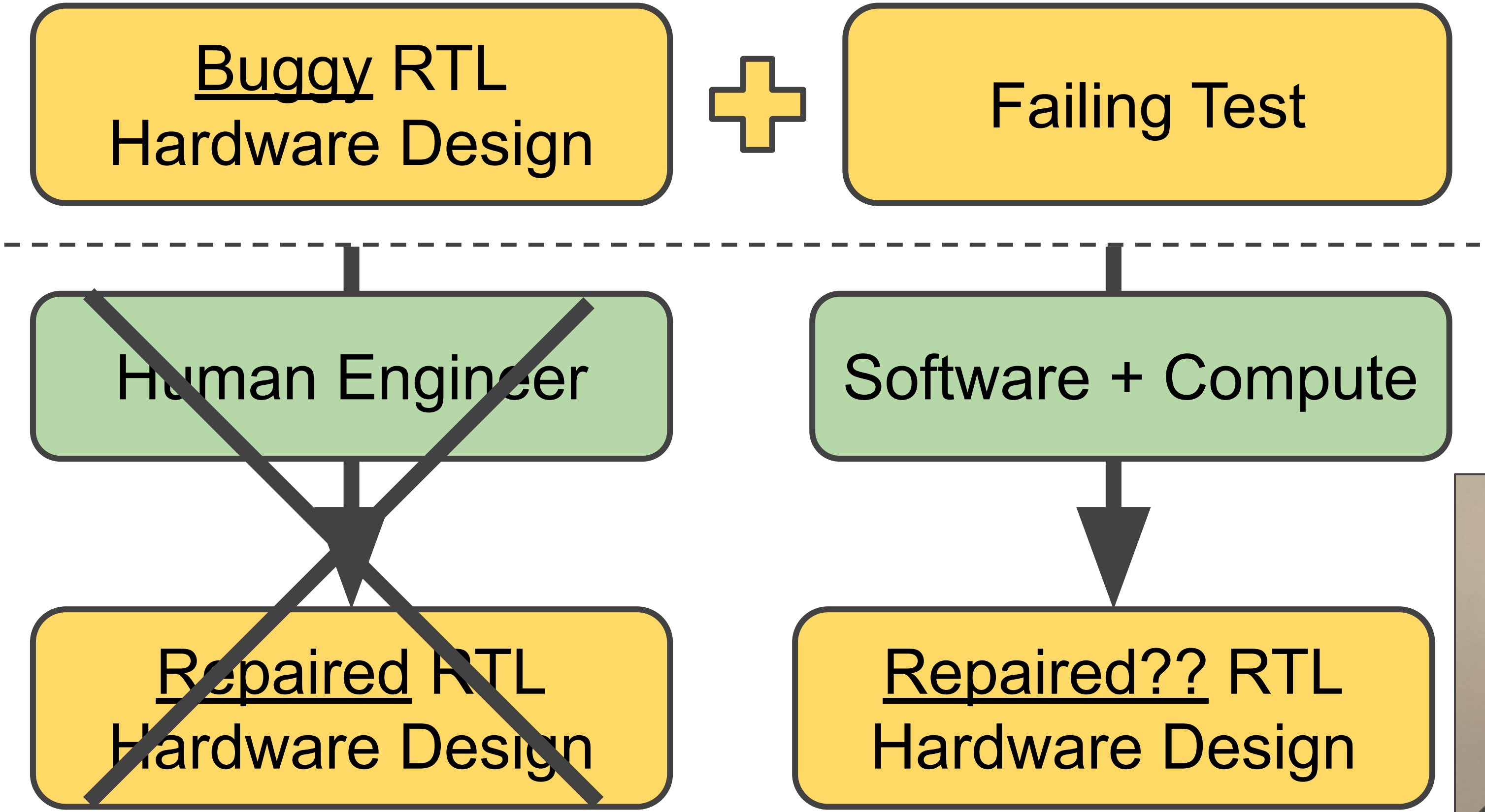
Buggy RTL Hardware Design

+

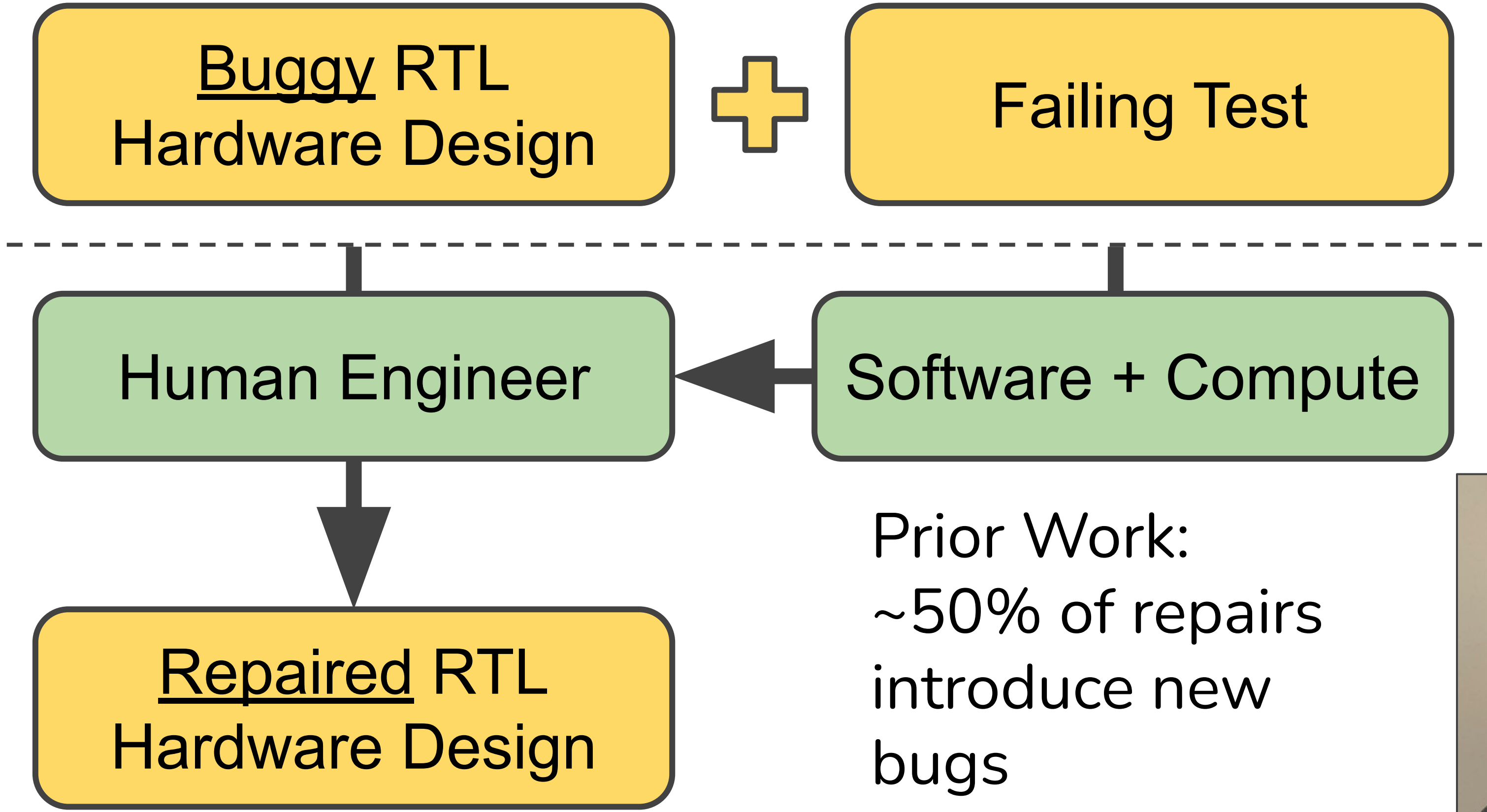
Failing Test


Buggy RTL Hardware Design
Failing Test
Human Engineer
Repaired RTL Hardware Design

## Automated Program Repair

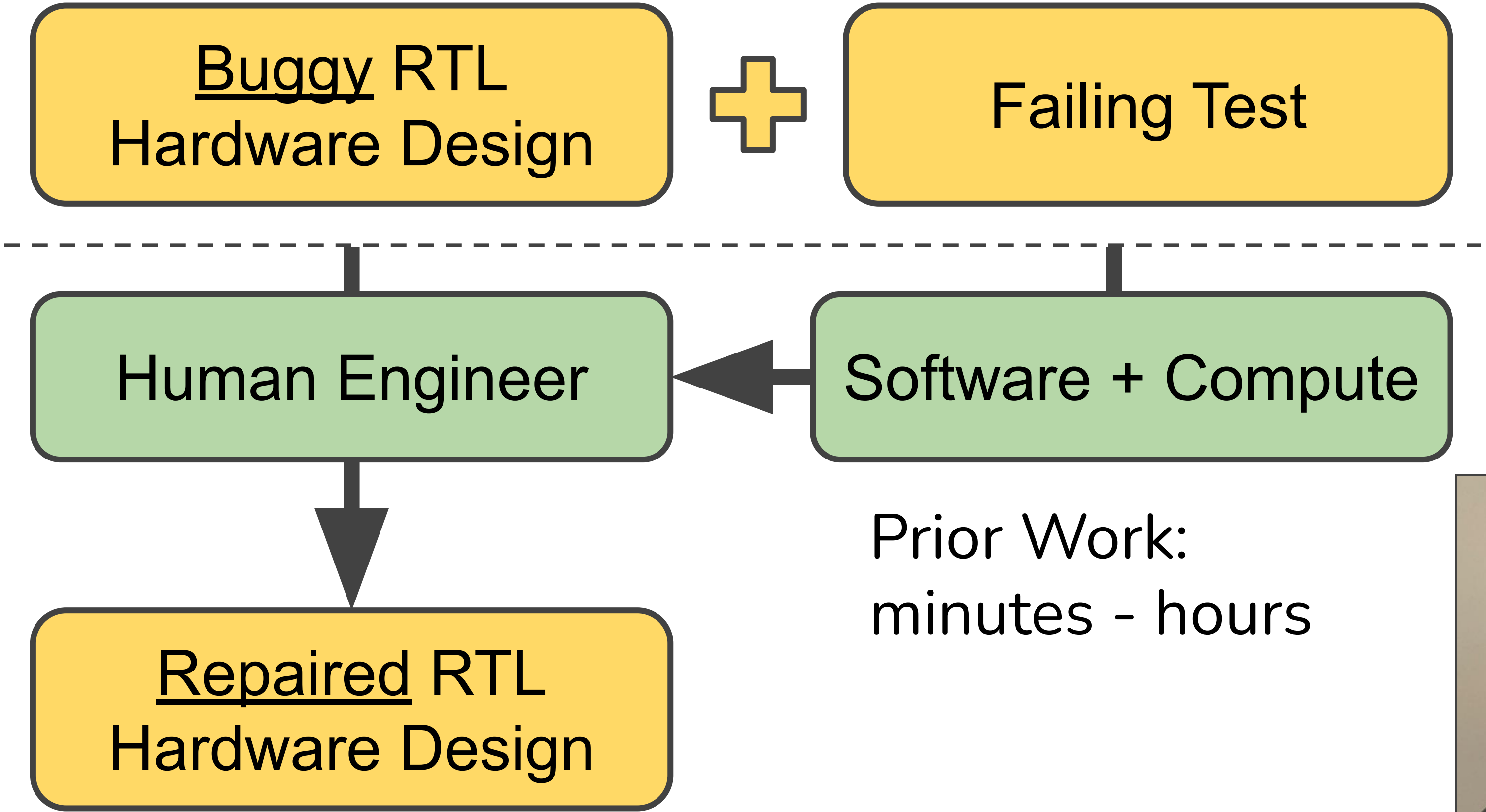

Buggy RTL Hardware Design
Failing Test
Human Engineer
Software + Compute
Repaired RTL Hardware Design
Repaired?? RTL Hardware Design

## Automated Program Repair



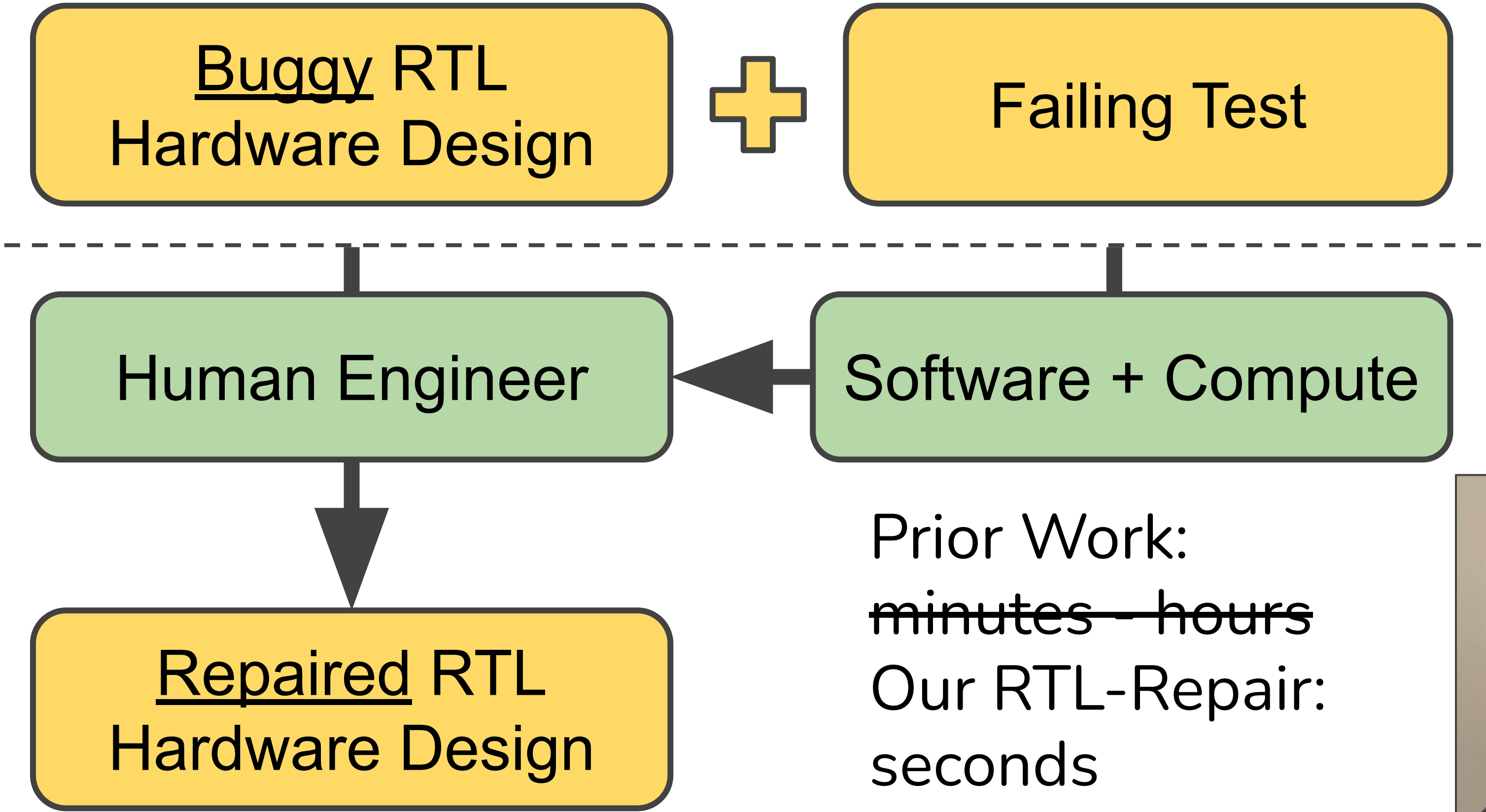
Prior Work:
~50% of repairs introduce new bugs

## Automated Program Repair



Prior Work:
minutes - hours

## Automated Program Repair



Prior Work:
~~minutes - hours~~
Our RTL-Repair:
seconds

## RTL-Repair

```
module counter(....);
always@(posedge clock) begin
 if(reset) begin
   overflow <= 1'b0;
   count <= 4'b0;
 end else if(enable) begin
   count <= count + 1;
 end
 if(count == 'd1) begin
   overflow <= 1'b1;
 end
end
endmodule
```

## RTL-Repair

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 end
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```

| reset | enable | count | overflow |
|---|---|---|---|
| 1 |  | x | x |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 |

## RTL-Repair

```
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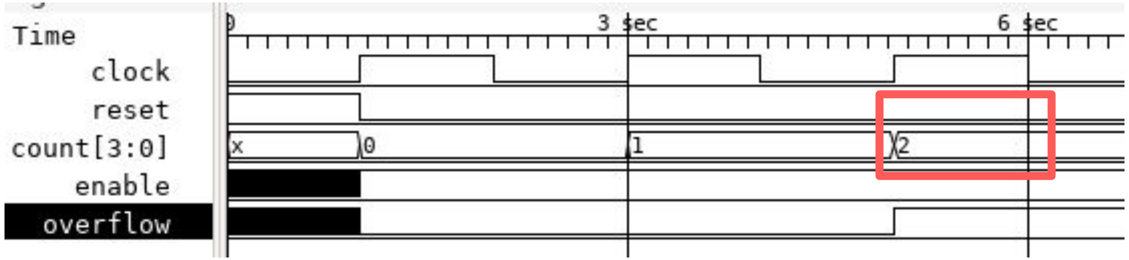

❌ count@3: 2 != 0 (expected)

| reset | enable | count | overflow |
|---|---|---|---|
| 1 | | x | x |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | **0** | 1 |

## RTL-Repair

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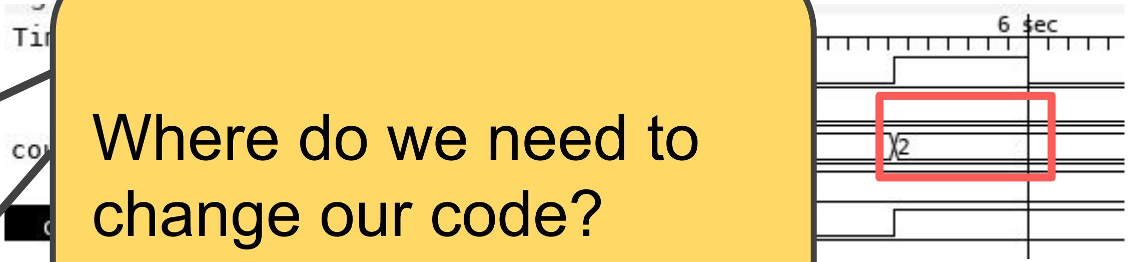

Where do we need to change our code?

xpected)

| reset | enable | count | overflow |
|---|---|---|---|
| 1 |  | x | x |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | **0** | 1 |

## RTL-Repair

```
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 end
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 end
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```

**After 1s on my laptop:**
*Add the following:*

```
count <= 4'b0;
```

xpected)

| reset | enable | count | overflow |
|---|---|---|---|
| 1 |  | x | x |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | **0** | 1 |

## RTL-Repair

```
module counter(....);
always@(posedge clock) begin
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| reset | enable | count | overflow |
|---|---|---|---|
| 1 |  | x | x |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | **0** | 1 |

## RTL-Repair

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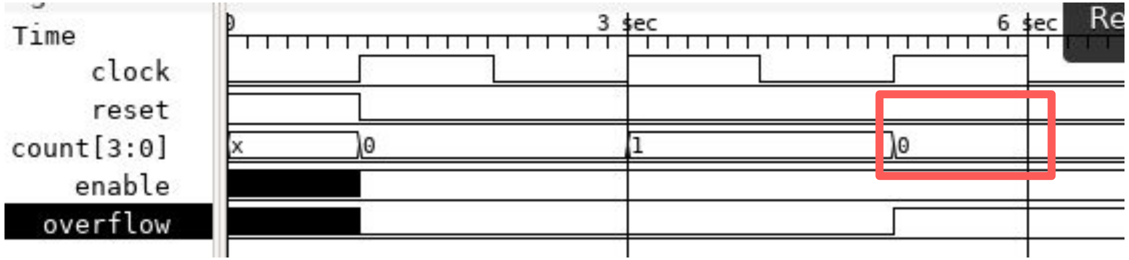

✓

| reset | enable | count | overflow |
|---|---|---|---|
| 1 | | x | x |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | **0** | 1 |

| | RTL-Repair | | | CirFix [6] | | |
|---|---|---|---|---|---|---|
| | # | median | max | # | median | max |
| ✔ Correct Repairs | 16 | 0.70s | 13.17s | 10 | 2.53min | 14.19h |
| ✖ Wrong Repairs | 2 | 0.51s | 0.68s | 11 | 2.03h | 9.50h |
| ○ Cannot Repair | 14 | 5.64s | 59.81s | 11 | 16.00h | 16.00h |

| | RTL-Repair | | | CirFix [6] | | |
|---|---|---|---|---|---|---|
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| ○ Cannot Repair | 14 | 5.64s | 59.81s | 11 | 16.00h | 16.00h |

# RTL-Repair: Fast Symbolic Repair of Hardware Design Code

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[Paper PDF]

[Code on Github]

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